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What is claimed is:

1. A video code processing method, comprising:

(a) providing a first original bit stream including a video code which is a digitized video signal;

(b) generating a second original bit stream at a first timing by delaying said first original bit stream by a specific time interval;

(c) generating a converted bit stream at a second timing, said first original bit stream being code-converted into said converted bit stream; and

(d) switching between said second original bit stream and said converted bit stream to output, and

wherein said specific time interval is adjusted such that said first timing is substantially equal to said second timing.

2. A video code processing method according to Claim 1, wherein said specific time interval is adjusted such that continuous moving pictures corresponding to said first original bit stream can be obtained even when said (d) is performed in a course of said second original bit stream and said converted bit stream.

3. A video code processing method according to Claim 1, wherein each of said second original bit stream and said converted bit stream has a plurality of frames, and

wherein said (d) includes switching between said second original bit stream and said converted bit stream at a switching point corresponding to a start position or end position of one of said plurality of frames of said second original bit stream and said converted bit stream.

4. A video code processing method according to Claim 1, wherein said first timing is determined by monitoring said second timing and controlling said specific time interval based on the monitoring result.

5. A video code processing method according to Claim 1, wherein said first timing is determined by monitoring said first and second timings and controlling said specific time interval based on the monitoring result.

6. A video code processing method according to Claim 5, wherein said first timing is determined by monitoring said first and second timings and performing feedback control on said specific time

interval such that a difference between said first and second timings is reduced based on the monitoring result.

7. A video code processing method according to Claim 1, wherein said (d) includes switching between said second original bit stream and said converted bit stream at a switching point detected in accordance with a bit stream structure of an encoded picture of said first original bit stream.

8. A video code processing method according to Claim 7, wherein said switching point is detected in accordance with a bit stream structure of an encoded picture of said first original bit stream such that continuous moving pictures corresponding to said first original bit stream can be obtained without a disturbance in said continuous moving pictures.

9. A video code processing method according to Claim 1, further comprising:

(f) inputting a switch command at a third timing, and

wherein each of said second original bit stream and said converted bit stream corresponds to MPEG (Moving Picture Experts Group) 2 type and

has a plurality of GOPs (Group of Picture), each of said plurality of GOPs including an Intra-Picture (I Picture), a Predictive-Picture (P picture) and a Bidirectionally predictive-Picture (B picture), and

wherein said (d) includes switching between said second original bit stream and said converted bit stream at a switching point corresponding to a lead position of one of said plurality of GOPs which is on said third timing or the closest to said third timing after said third timing.

10. A video code processing apparatus, comprising:

a buffer section inputting a first original bit stream including a video code which is a digitized video signal to generate a second original bit stream at a first timing by delaying said first original bit stream by a specific time interval;

a transcoding section generating a converted bit stream at a second timing, said first original bit stream being code-converted into said converted bit stream; and

a switching section switching between said second original bit stream and said converted bit stream to output, and

wherein said specific time interval is adjusted such that said first timing is substantially equal to said second timing.

11. A video code processing apparatus according to Claim 10, wherein said specific time interval is adjusted such that continuous moving pictures corresponding to said first original bit stream can be obtained even when said switching section switches between said second original bit stream and said converted bit stream in a course of said second original bit stream and said converted bit stream.

12. A video code processing apparatus according to Claim 11, wherein each of said second original bit stream and said converted bit stream has a plurality of frames, and

wherein said switching section switches between said second original bit stream and said converted bit stream at a switching point corresponding to a start position or end position of one of said plurality of frames of said second original bit stream and said converted bit stream.

13. A video code processing apparatus according to Claim 10, further comprising:

a buffer controlling section monitoring said second timing to control said specific time interval based on the monitoring result.

14. A video code processing apparatus according to Claim 10, further comprising:

a buffer controlling section monitoring said first and second timings to control said specific time interval based on the monitoring result.

15. A video code processing apparatus according to Claim 10, further comprising:

a buffer controlling section monitoring said first and second timings to perform feedback control on said specific time interval such that a difference between said first and second timings is reduced based on the monitoring result.

16. A video code processing apparatus according to Claim 10, wherein said switching section switches between said second original bit stream and said converted bit stream at a switching point detected in accordance with a bit stream structure of an encoded picture of said first original bit stream.

17. A video code processing apparatus according to Claim 10, further comprising:

a switch controlling section inputting a switch command at a third timing to determine a switching point at which said switching section switches between said second original bit stream and said converted bit stream, and

wherein each of said second original bit stream and said converted bit stream corresponds to MPEG (Moving Picture Experts Group) 2 type and has a plurality of GOPs (Group of Picture), each of said plurality of GOPs including an Intra-Picture (I Picture), a Predictive-Picture (P picture) and a Bidirectionally predictive-Picture (B picture), and

wherein said switch controlling section determines said switching point such that said switching point corresponds to a lead position of one of said plurality of GOPs which is on said third timing or the closest to said third timing after said third timing.

18. A video code processing apparatus according to Claim 10, wherein said buffer section and said transcoding section and said switching section are included in a single unit.

19. A video code processing apparatus according to Claim 13, wherein said buffer section and said transcoding section and said switching section and said buffer controlling section are included in a single unit.

20. A video code processing apparatus according to Claim 17, wherein said buffer section and said transcoding section and said switching section and said buffer controlling section and said switch controlling section are included in a single unit.